LISTING OF CLAIMS

1. (Original) A detection circuit for detecting whether a signal is oscillating, comprising:

first detect circuitry, comprising:

at least one capacitive element;

a first circuit for placing, at a first drive strength, a first voltage across the at least one capacitive element; and

a second circuit for selectively placing, at a second drive strength greater than the first drive strength, a second voltage across the at least one capacitive element when activated, the second circuit being coupled to receive the signal and being activated based upon a value of the signal; and

an output circuit having an input coupled to the capacitive element and having an output having a value based upon the voltage appearing across the capacitive element.

2. (Original) The detection circuit of claim 1, wherein the first voltage is a voltage representative a first logic value and the second voltage is a voltage representative of a second logic value.

3. (Original) The detection circuit of claim 1, wherein the first logic value is a logic high value and the second logic value is a logic low value.

4. (Original) The detection circuit of claim 1, wherein the first circuit comprises a current source for sourcing current to the at least one capacitive element.

5. (Original) The detection circuit of claim 4, wherein the current source comprises at least a portion of a current mirror having a first current leg and a second current leg coupled to the at least one capacitive element.

6. (Original) The detection circuit of claim 4, wherein the second circuit comprises a transistor coupled across the at least one capacitive element, a control terminal of the transistor being coupled to the signal.

7. (Original) The detection circuit of claim 6, wherein the transistor of the second circuit is sized larger than the size of transistors in the second current leg of the current mirror.

8. (Original) The detection circuit of claim 6, further comprising a third circuit for initially placing the second voltage across the at least one capacitive element when enabled.

9. (Original) The detection circuit of claim 1, wherein the second circuit comprises a Schmitt-trigger circuit having an input coupled to the at least one capacitive element and an output coupled to an input of the output circuit.

10. (Original) The detection circuit of claim 1, further comprising:

second detect circuitry, comprising:

at least one capacitive element;

a first circuit for placing, at a third drive strength, one of the first and second voltages across the at least one capacitive element of the second detect circuitry; and

a second circuit for selectively placing, at a fourth drive strength greater than the third drive strength, the other of the first and second voltages across the at least one capacitive element of the second detect circuitry when activated, the second circuit of the second detect circuitry being coupled to receive the signal and being activated based upon a value of the signal, the at least one capacitive element of the second detect circuitry being coupled to an input of the output circuit so that the output of the output circuit is based in part upon a voltage appearing across the at least one capacitive element of the second detect circuitry.

11. (Original) The detection circuit of claim 10, wherein the signal activates the second circuit of the first detect circuitry when in a first logic state and activates the second circuit of the second detect circuitry when in a second logic state different from the first logic state.

12. (Original) The detection circuit of claim 10, further comprising circuitry for initially placing the first voltage across both of the at least one capacitive elements when activated.

13. (Original) The detection circuit of claim 10, wherein the first drive strength is substantially the same as the third drive strength, and the second drive strength is substantially the same as the fourth drive strength.

14. (Original) A method for detecting whether a signal is oscillating between at least two logic states, comprising:

initially placing a first voltage level across at least one first capacitive element;

driving, with a first drive strength, a voltage appearing across the at least one first capacitive element towards a second voltage level;

selectively driving, with a second drive strength greater than the first drive strength, the voltage across the at least one first capacitive element towards the first voltage level when the signal is in a first of the at least two logic states; and

generating an output signal having a value based upon a voltage level across the at least one first capacitive element.

15. (Original) The method of claim 14, wherein the first voltage level corresponds to a logic low value and the second voltage level corresponds to a logic high value.

16. (Original) The method of claim 14, wherein the second voltage level corresponds to a logic low value and the first voltage level corresponds to a logic high value.

17. (Original) The method of claim 14, wherein the output signal switches between first and second logic states based upon the voltage appearing across the at least one first capacitive element relative to a predetermined voltage between the first voltage level and the second voltage level.

18. (Original) The method of claim 14, further comprising:

initially placing a third voltage level across at least one second capacitive element;

driving, with a third drive strength, a voltage appearing across the at least one second capacitive element towards a fourth voltage level;

selectively driving, with a fourth drive strength greater than the third drive strength, the voltage across the at least one second capacitive element towards the third voltage level when the signal is in a second of the at least two logic states, wherein the output signal has a value based upon a voltage level across the at least one second capacitive element.

19. (Original) The method of claim 18, wherein the first voltage level is approximately equal to the third voltage level and the second voltage level is approximately equal to the fourth voltage level.

20. (Original) The method of claim 18, wherein the first voltage level is approximately equal to the fourth voltage level and the second voltage level is approximately equal to the third voltage level.

21. (Original) The method of claim 18, wherein the third drive strength is substantially the same as the first drive strength, and the fourth drive strength is substantially the same as the second drive strength.

22. (Currently Amended) An apparatus, comprising:

a first circuit that generates an output signal; and

a second circuit having an input coupled to the output signal of the first circuit, the second circuit detecting whether the output signal of the first circuit oscillates at a frequency that is less than a predetermined frequency ~~, the second circuit capable of~~ by determining whether the output signal ~~of the first circuit~~ remains in one of a first or second logic state in excess of ~~for at least~~ a predetermined period of time ~~and in a second logic state for at least the predetermined period of time~~.

23. (Currently Amended) An apparatus, comprising:

a first circuit that generates an output signal; and

a second circuit having an input coupled to the output signal of the first circuit, the second circuit detecting whether the output signal of the first circuit oscillates at a frequency that is less than a predetermined frequency, the second circuit capable of determining whether the output signal of the first circuit remains in a first logic state for at least a predetermined period of time or in a second logic state for at least the predetermined period of time;

~~The apparatus of claim 22,~~ wherein the second circuit comprises:

a first capacitive element;

a third circuit for charging the first capacitive element towards a first voltage level;

a fourth circuit for selectively charging the first capacitive element towards a second voltage level at a drive strength greater than a drive strength at which the third circuit charges the first capacitive element, the fourth circuit being activated when the output signal of the first circuit is in the first logic state; and

a fifth circuit having an input coupled to the first capacitive element for generating an output signal having a value dependent upon the voltage appearing across the first capacitive element.

24. (Original) The apparatus of claim 23, wherein the first voltage level corresponds to a logic low state and the second voltage level corresponds to a logic high state.

25. (Original) The apparatus of claim 23, wherein the first voltage level corresponds to a logic high state and the second voltage level corresponds to a logic low state.

26. (Original) The apparatus of claim 23, further comprising:

a second capacitive element;

a sixth circuit for charging the second capacitive element towards a third voltage level;

a seventh circuit for selectively charging the second capacitive element towards a fourth voltage level at a drive strength greater than a drive strength at which the sixth circuit charges the second capacitive element, the seventh circuit being activated when the output signal of the first circuit is in the second logic state, the value of the output signal of the fifth circuit being based upon the voltage level appearing across the second capacitive element.

27. (Original) The apparatus of claim 26, wherein the first voltage level is substantially the same as the third voltage level and the second voltage level is substantially the same as the fourth voltage level.

28. (Original) The apparatus of claim 26, wherein the first voltage level is substantially the same as the fourth voltage level and the second voltage level is substantially the same as the third voltage level.

29. (Original) The apparatus of claim 26, wherein the sixth circuit comprises at least a portion of a current mirror.

30. (Original) The apparatus of claim 23, wherein the third circuit comprises at least a portion of a current mirror.

31. (Original) The apparatus of claim 23, wherein the first voltage level corresponds to a logic high state and the second voltage level corresponds to a logic low state.

32. (New) The apparatus of claim 22 wherein the second circuit comprises:

a charging circuit that charges a capacitor in response to the output signal being in one of the first or second logic states;

a discharging circuit that discharges the capacitor in response to transition of the output signal to the other of the first or second logic states; and

a capacitor voltage detection circuit measuring a voltage stored on the capacitor, the measured voltage being indicative of whether the output signal remains in one of a first or second logic state in excess of a predetermined period of time.

33. (New) The apparatus of claim 32,

wherein the charging circuit comprises:

a capacitive element; and

a current source for charging the capacitive element towards a first reference voltage; and

wherein the discharging circuit comprises:

a switching circuit for selectively discharging the capacitive element towards a second reference voltage, the switching circuit being activated in response to output signal transition.

34. (New) The apparatus of claim 22, wherein the first voltage level corresponds to a logic low state and the second voltage level corresponds to a logic high state.